STIC Search Report
EIC 2100

STIC Database Tracking Number: 157340

TO:	From:
Jean Fleurantin **Location: 3B29** **Art Unit : 2162** **Thursday, June 23, 2005** **Case Serial Number: 09/229849**	**David Holloway** **Location: EIC 2100** **RND 4B19** **Phone: 2-3528** **david.holloway@uspto.gov**

Search Notes

Dear Examiner Fleurantin,

Attached please find your search results for above-referenced case.
Please contact me if you have any questions or would like a re-focused search.

David

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Set     Items   Description
S1     101451   (CLUSTER OR PARALLEL?)(N)(COMPUTER OR COMPUTERS OR PROCESS-
             OR?) OR MMP  OR SHARED()MEMOR? OR MASPAR OR SIMD OR MP()(1 OR
             2 OR ONE OR TWO)
S2    3192591   SCRIPT? OR TOOL? ? OR AGENT? OR MACRO OR MACROS OR JAVA OR
             JSCRIPT OR JAVASCRIPT OR APPLET OR JVSCRIPT OR ACTIVEX OR ACT-
             IVE()X OR SCENARIO? OR INSTRUCTION(N)(SET OR SETS)
S3     488428   PARSE? OR PARSING OR REPARS? OR MAP OR MAPPING MAPS OR MAP-
             PED OR TOKENI?
S4      65092   (GENERAT? OR BUILD? OR ASSEMBL? OR CREAT? OR WRITE OR REWR-
             IT? OR CLONE? OR REPLICAT? OR DUPLICAT? OR REPRODUC?)(3N)S2
S5        308   S1 AND S4
S6         13   S3 AND S5
S7         39   S2(3N)S3 AND S1
S8         34   S1(5N)S4
S9         85   S6:S8
S10        58   S9 NOT PY>1999
S11        35   RD (unique items)
File   8:Ei Compendex(R) 1970-2005/Jun W2
         (c) 2005 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2005/May
         (c) 2005 ProQuest Info&Learning
File  65:Inside Conferences 1993-2005/Jun W3
         (c) 2005 BLDSC all rts. reserv.
File   2:INSPEC 1969-2005/Jun W2
         (c) 2005 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2005/May W1
         (c)2005 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Jun 23
         (c) 2005 The Gale Group
File   6:NTIS 1964-2005/Jun W2
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2005/Jun W2
         (c) 2005 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2005/Jun W3
         (c) 2005 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/May
         (c) 2005 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2005/May W3
         (c) 2005 FIZ TECHNIK
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11/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04862243 E.I. No: EIP97103904600
Title: Incorporating application dependent information in an automatic code generating environment
Author: van Engelen, Robert; Heitlager, Ilja; Wolters, Lex; Cats, Gerard
Corporate Source: Leiden Univ, Leiden, Neth
Conference Title: Proceedings of the 1997 International Conference on Supercomputing
Conference Location: Vienna, Austria Conference Date: 19970707-19970711
Sponsor: ACM
E.I. Conference No.: 47178
Source: Proceedings of the International Conference on Supercomputing 1997. ACM, New York, NY, USA. p 180-187
Publication Year: 1997
CODEN: 002151
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9712W4
Abstract: In this paper, we demonstrate the necessity of including high-level information for automatic generation of efficient codes for serial, vector, and **parallel computer** architectures with the CTADEL code **generation tool** . The CTADEL Code- **generation Tool** for Applications based on Differential Equations using high-level Language specifications is a programming environment developed for the generation of efficient codes for PDE-based problems. The tool has been adopted as an application driver for the HIRLAM numerical weather forecast system. More specifically, we present a framework for high-level code restructuring based on monotonicity information about the data structures used. This information is not available in state-of-the-art vectorizing and parallelizing compilers but it is of vital importance for the generation of efficient architecture-specific codes. The performance of the generated codes for a typical example problem encountered in the so-called physics routines of the HIRLAM system are compared to the hand-written production code. The performance results demonstrate the usefulness of the presented technique. (Author abstract) 13 Refs.
Descriptors: *Codes (symbols); High level languages; Parallel processing systems; Computer architecture; Partial differential equations; Computer programming; Data structures; Program compilers; Mathematical models
Identifiers: Automatic code generation; Software Package CTADEL; Physics routines; HIRLAM numerical weather forecast system
Classification Codes:
723.1.1 (Computer Programming Languages)
723.2 (Data Processing); 723.1 (Computer Programming); 722.4 (Digital Computers & Systems); 921.2 (Calculus); 921.6 (Numerical Methods)
723 (Computer Software); 722 (Computer Hardware); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

11/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04702236 E.I. No: EIP97053665851
Title: HPFIT: A set of integrated tools for the parallelization of applications using High Performance Fortran. Part I: HPFIT and the TransTOOL environment
Author: Brandes, T.; Chaumette, S.; Counilh, M.C.; Roman, J.; Darte, A.; Desprez, F.; Mignot, J.C.
Corporate Source: German Natl Research Cent for Computer Science, St. Augustin, Ger
Conference Title: Proceedings of the 1996 International Workshop on Environments and Tools for Parallel Scientific Computing
Conference Location: Faverges de la Tour, Fr Conference Date: 19960822-19960823
E.I. Conference No.: 46398
Source: Parallel Computing v 23 n 1-2 Apr 1997. p 71-87
Publication Year: 1997
CODEN: PACOEJ ISSN: 0167-8191
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); G; (General Review)
Journal Announcement: 9707W3
Abstract: In this paper, we present the HPFIT project whose aim is to provide a set of interactive tools integrated in a single environment to help users to parallelize scientific applications to be run on distributed memory **parallel computers** . HPFIT is built around a restructuring tool called TransTOOL which includes an editor, a **parser** , a dependence analysis **tool** and an optimization kernel. Moreover, we provide a clean interface to help developers of tools around High Performance Fortran to integrate their software within our tool. (Author abstract) 37 Refs.
Descriptors: *Parallel processing systems; Computer architecture; Percolation (computer storage); Optimization; FORTRAN (programming language); Computer software; Interactive computer systems; User interfaces ; Storage allocation (computer); Computer aided software engineering
Identifiers: Software package TransTOOL
Classification Codes:
723.1.1 (Computer Programming Languages)
722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 921.5 (Optimization Techniques); 723.1 (Computer Programming); 722.2 (Computer Peripheral Equipment)
722 (Computer Hardware); 723 (Computer Software); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

11/5/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04491316 E.I. No: EIP96093325335
Title: Optimizing parallel program execution by self-organizing maps
Author: Quittek, Juergen W.
Corporate Source: Technical Univ of Hamburg, Hamburg, Ger
Source: Journal of Artificial Neural Networks v 2 n 4 1995. p 365-380
Publication Year: 1995
CODEN: JANNE5 ISSN: 1073-5828
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9611W1
Abstract: A complex problem in parallel processing is called the mapping problem. The parts of a parallel program are to be **mapped** to components of a **parallel computer** such that the total program execution time becomes minimal. This paper presents self-organizing feature maps as an efficient **tool generating** solutions of the mapping problem. Parallel program and **parallel computer** are modeled by graphs. Based on the Kohonen learning rule some adaptations are necessary to apply self-organizing maps. Special metrics reflecting properties of the parallel program respectively the **parallel computer** allows to **map** arbitrary parallel programs onto most of the common parallel architectures (two-dimensional lattice, three-dimensional torus, hypercube, etc.). Simulations and applications to reference problems show that self-organizing maps are more efficient than other optimizing methods (e.g. Simulated Annealing) applied to this NP-hard problem. (Author abstract) 17 Refs.
Descriptors: *Neural networks; Parallel processing systems; Optimization; Computer systems programming; Computer architecture; Graph theory; Learning systems; Computer simulation; Computational complexity; Problem solving
Identifiers: Self organizing maps; Load balancing; Kohonen learning rule; Parallel programs
Classification Codes:
723.4 (Artificial Intelligence); 722.4 (Digital Computers & Systems); 921.5 (Optimization Techniques); 723.1 (Computer Programming); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 723.5 (Computer Applications)
723 (Computer Software); 722 (Computer Hardware); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

11/5/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03817039 E.I. No: EIP94031233493
Title: Automating data conversion for heterogeneous distributed shared memory
Author: Wortman, D.B.; Zhou, S.; Fink, S.
Corporate Source: Univ of Toronto, Toronto, Ont, Can
Source: Software - Practice and Experience v 24 n 1 Jan 1994. p 111-125
Publication Year: 1994
CODEN: SPEXBL ISSN: 0038-0644
Language: English
Document Type: JA; (Journal Article) Treatment: T; (Theoretical)
Journal Announcement: 9404W5
Abstract: This paper describes the issues involved in sharing data among processes executing co-operatively in a heterogeneous computing environment. In a heterogeneous environment, the physical representation of a data object may need to be transformed when the object is moved from one type of processor to another. As a part of a larger project to build a heterogeneous distributed **shared memory** system we developed an automated **tool** for **generating** the conversion routines that are used to implement representation conversion for data objects. We developed a novel method for processing source programs that allowed us to extract detailed information about the physical representation of data objects without access to the source code of the compilers that were generating those representations. A performance comparison with the more general XDR heterogeneous data conversion package shows that the customized conversion routines that we generate are 4 to 8 times faster. (Author abstract) 12 Refs.
Descriptors: *Data processing; Automation; Analog to digital conversion; Digital to analog conversion; Data handling; Distributed computer systems; Object oriented programming; Data structures; Computer software; Virtual storage
Identifiers: Data objects; Heterogeneity; External data representation; Automatic data conversion; XDR; Mermaid
Classification Codes:
723.2 (Data Processing); 731.2 (Control System Applications); 722.4 (Digital Computers & Systems); 723.1 (Computer Programming); 722.3 (Data Communication, Equipment & Techniques); 722.1 (Data Storage, Equipment & Techniques)
723 (Computer Software); 731 (Automatic Control Principles); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 73 (CONTROL ENGINEERING)

11/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02794855 E.I. Monthly No: EIM8909-033212
Title: Software tool for the automatic generation of memory traces for shared memory multiprocessor systems.
Author: Gupta, Saurabh; Melhem, Rami
Corporate Source: Cap Gemini America, Cranford, NJ, USA
Conference Title: Record of Proceedings: the 22nd Annual Simulation Symposium
Conference Location: Tampa, FL, USA Conference Date: 19890328
Sponsor: Assoc for Computing Machinery, New York, NY, USA; Int Assoc for Mathematics and Computers in Simulation, Brussels, Belg
E.I. Conference No.: 12373
Source: Rec Proc 22th Annu Simul Symp Record of Proceedings - Annual Simulation Symposium 22nd. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2740-9), Piscataway, NJ, USA. p 93-104
Publication Year: 1989
CODEN: RASSDU ISSN: 0272-4715
Language: English
Document Type: PA; (Conference Paper) Treatment: T; (Theoretical)
Journal Announcement: 8909
Abstract: A software tool that allows for the simulation of parallel programs on shared-memory, multiple-instruction/multiple-data (MIMD) machines in the absence of such a machine, is described. The purpose is to obtain a history of requests generated by parallel programs to the shared memory. Specifically, the result of the simulation is a memory trace which records the history of memory access. The trace contains information such as the time of the request, the identification of the processor making the request, and the specific memory location accessed. The software tool consists of a translator-augmenter which translates and enhances programs written in a parallel version of C into standard C programs, called trace generators. When compiled and executed as C programs, the trace generators generate static memory traces. These traces can be used to simulate and analyze memory contentions in different memory architectures and to evaluate and compare different parallel algorithms. 9 refs.
Descriptors: *COMPUTER SYSTEMS, DIGITAL--*Multiprocessing; DATA STORAGE, DIGITAL; COMPUTER OPERATING SYSTEMS--Program Translators; COMPUTER PROGRAMMING--Algorithms; COMPUTER SIMULATION
Identifiers: MEMORY TRACES; SHARED MEMORY; PARALLEL PROGRAMS; MEMORY ACCESS; TRANSLATOR-AUGMENTER
Classification Codes:
722 (Computer Hardware); 723 (Computer Software); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)

11/5/10 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02283139 E.I. Monthly No: EIM8710-072701
Title: TRANSFORMING CONCURRENT ALGORITHMS FOR DIFFERENT PARALLEL ARCHITECTURES.
Author: Gannon, Dennis; Wang, Ko-Yang
Corporate Source: Indiana Univ, Bloomington, IN, USA
Conference Title: Proceedings of the Twentieth Hawaii International Conference on System Sciences 1987. (Volume 1: Architecture, Decision Support Systems and Knowledge-Based Systems.)
Conference Location: Kailua-Kona, HI, USA Conference Date: 19870106
Sponsor: Univ of Hawaii, Honolulu, HI, USA; Univ of Southwestern Louisiana, Lafayette, LA, USA; ACM, New York, NY, USA; IEEE Computer Soc, Technical Committee on Computational Medicine, Los Alamitos, CA, USA
E.I. Conference No.: 10229
Source: Proceedings of the Hawaii International Conference on System Science 20th v 1. Publ by Western Periodicals Co, North Hollywood, CA, USA p 134-141
Publication Year: 1987
CODEN: PHISD7 ISSN: 0073-1129
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8710
Abstract: This paper describes a project to **build** software **tools** for aiding in the process of moving parallel algorithms from one machine to another. In particular, we illustrate the different sequences of program transformations needed to **map** algorithms to three different machines. These include the Alliant FX/8, the BBN Butterfly and a 64 processor non-**shared memory** (configurable systolic) array. (Author abstract) 17 refs.
Descriptors: *COMPUTER SYSTEMS, DIGITAL--*Parallel Processing; COMPUTER PROGRAMMING--Algorithms; COMPUTER ARCHITECTURE; COMPUTER SOFTWARE
Identifiers: CONCURRENT ALGORITHMS; NON- **SHARED MEMORY**
Classification Codes:
722 (Computer Hardware); 723 (Computer Software); 713 (Electronic Circuits); 714 (Electronic Components)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

01144360 ORDER NO: AAD91-05386

BOUNDARY SURFACES OF TOOL SWEPT VOLUMES USING MASSIVELY PARALLEL ALGORITHMS

Author: YUNG, YEE TAK
Degree: PH.D.
Year: 1991
Corporate Source/Institution: BOSTON UNIVERSITY (0017)
Major Professor: MERRILL L. EBNER
Source: VOLUME 51/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4569. 219 PAGES
Descriptors: ENGINEERING, MECHANICAL; ENGINEERING, INDUSTRIAL; COMPUTER SCIENCE
Descriptor Codes: 0548; 0546; 0984

In NC machining, the result of the tool motion in machining a complex shape is often uncertain. Trials on actual NC machines are time consuming and costly. In principle, the material removal process can be modeled by the Boolean difference between the tool swept volume and the workpiece. One difficulty is the lack of a generalized mathematical basis for tool swept volumes. Another difficulty arises from the massive amount of data needed in the computation.

In this thesis, the formulation of swept volumes for rotational cutting tools undergoing 5-axis NC machining motions is developed. The tool swept volume is defined by its boundary which is a subset of the tool boundary during the motion. The tool boundary is represented by surfaces of revolution joined by circular edges. The tool motion is defined by the kinematics of the NC machine and the interpolation used to synchronize movements of machine axes between the initial and final positions. The Jacobian determinant in the parametric space, indicating the direction sense of the motion relative to the surface normal of the tool boundary is used to establish the necessary conditions for the boundary surfaces of tool swept volumes, which include: (1) envelopes of 1-parameter families of surfaces of revolution, (2) surfaces formed by 1-parameter families of circular edges, and (3) a subset of the initial and final instances of the tool boundary.

Massively parallel algorithms are developed and implemented on a **SIMD parallel computer** to: (1) **generate** boundary representations of **tool** swept volumes, (2) perform Boolean subtractions between boundary representations of the tool swept volume and the workpiece, and (3) render raster images of machined objects. A series of test cases, including four parts with spherical pockets, two propellers, and a detailed medallion, are simulated on the SIMD computer and machined on a 5-axis milling machine. In all cases, the computed models and machined parts are identical, demonstrating the correctness of the techniques.

11/5/17 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

00244991 INSIDE CONFERENCE ITEM ID: CN002253781
Program generating tools **for** parallel computer **DAP510 and its application to engineering problems**
Takagi, S.
CONFERENCE: Parallel computing in engineering and engineering education-1st World conference
WORLD CONFERENCE ON PARALLEL COMPUTING IN ENGINEERING AND ENGINEERING EDUCATION, 1990; 1st P: 205-210
London, The Microcomputer Unit, 1990
ISBN: 187306800X
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE SPONSOR: Unesco
CONFERENCE LOCATION: Paris
CONFERENCE DATE: Oct 1990 (199010) (199010)

BRITISH LIBRARY ITEM LOCATION: 9353.267420
DESCRIPTORS: parallel computing; engineering; engineering education; Unesco

11/5/19 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6071036 INSPEC Abstract Number: C9812-6185-003
Title: Simulation model design in physical environments
Author(s): Brauer, V.
Author Affiliation: Res. Center artec, Bremen Univ., Germany
Journal: Computer Graphics vol.30, no.4 p.55-6
Publisher: ACM,
Publication Date: Nov. 1996 Country of Publication: USA
CODEN: CGRADI ISSN: 0097-8930
SICI: 0097-8930(199611)30:4L.55:SMDP;1-3
Material Identity Number: C251-96004
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: In the design of technical products and processes, physical models play an important role for stimulating creative acts and for supporting communication in teams. In **parallel computer** based planning, **tools** are used to **create** numerically exact systems which can be viewed, analyzed, simulated, reproduced and modified in various ways. In this article, the concept of a real reality user interface (RR) is introduced, and an example application is presented. By creating logical links between physical and virtual objects during the moving phase of real artifacts, it is possible to work synchronously in both model worlds: the physical and the virtual. (5 Refs)
Subfile: C
Descriptors: CAD; digital simulation; user interfaces; virtual reality
Identifiers: simulation model design; technical product design; physical models; team communication; parallel computer based planning; real reality user interface; physical objects; virtual objects
Class Codes: C6185 (Simulation techniques); C6180 (User interfaces); C6130B (Graphics techniques)

11/5/23 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03861483 INSPEC Abstract Number: C91029977
Title: Compiler Compilers Workshop
Journal: Informatik, Informationen Reporte no.8
Publication Date: 1990 Country of Publication: West Germany
ISSN: 0233-2582
Conference Title: Compiler Compilers Workshop
Conference Date: 22-24 Oct. 1990 Conference Location: Schwerin, Germany
Language: English Document Type: Conference Proceedings (CP); Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: The following topics were dealt with: application development with the FNC-2 attribute grammar system; recursive ascent-descent **parsers** ; compilation for instruction **parallel processors** ; generator for production quality compilers; Rie and Jun; attributed ELL(1)- **parser** generator; STARLET: affix-based compiler compiler designed as a logic programming system; PAGODE: back end generator using attribute abstract syntaxes and term rewritings; hybrid top-down **parsing** ; computer-aided **building** of a compiler; **tool** box for compiler construction; tree-abiding interface for Ada; multilingual natural language understanding interface; annotated programming; compiler with scheduling for a specialized synchronous multiprocessor system; mixed dialogue control defined by an attribute grammar; MATE, metasystem with concurrent attribute evaluation; LALR compiler compiler for incremental **parsers** ; DCGs; efficient code generation from continuation semantics; optimizing directly executable LR **parsers** ; algorithmic debugging for imperative languages with side-effects; and SYS/3, software development tool.
Subfile: C
Descriptors: grammars; program compilers
Identifiers: application development; FNC-2 attribute grammar system; recursive ascent-descent **parsers** ; instruction **parallel processors** ; production quality compilers; Rie; Jun; attributed ELL(1)- **parser** generator; STARLET; affix-based compiler compiler; logic programming system ; PAGODE; back end generator; attribute abstract syntaxes; term rewritings; hybrid top-down **parsing** ; computer-aided building; tool box; tree-abiding interface; Ada; multilingual natural language understanding interface; annotated programming; scheduling; specialized synchronous multiprocessor system; mixed dialogue control; attribute grammar; MATE; metasystem; concurrent attribute evaluation; LALR compiler compiler; incremental **parsers** ; DCGs; efficient code generation; continuation semantics; directly executable LR **parsers** ; algorithmic debugging; imperative languages; side-effects; SYS/3; software development tool
Class Codes: C6150C (Compilers, interpreters and other processors); C4210 (Formal logic)

11/5/28 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

03246492 INSPEC Abstract Number: C88063998
Title: An open environment for building parallel programming systems0
Author(s): Bershad, B.N.; Lazowska, E.D.; Levy, H.M.; Wagner, D.B.
Author Affiliation: Dept. of Comput. Sci., Washington Univ., Seattle, WA, USA
Journal: SIGPLAN Notices vol.23, no.9 p.1-9
Publication Date: Sept. 1988 Country of Publication: USA
CODEN: SINODQ ISSN: 0362-1340
Conference Title: ACM/SIGPLAN PPEALS 1988 - Parallel Programming: Experience with Applications, Languages and Systems
Conference Sponsor: ACM
Conference Date: 19-21 July 1988 Conference Location: New Haven, CT, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: PRESTO is a set of **tools** for **building** parallel programming systems on **shared - memory** multiprocessors. PRESTO's goal is to provide a framework within which one can easily build efficient support for any of a wide variety of 'models' of parallel programming. PRESTO is designed for easy modification and extension, not only at the level of the primitives and structures made available for the application programmer's use, but also at the level of the run-time kernel that supports parallel applications. PRESTO is implemented in the object-oriented language C++ on a Sequence Balance 21000 and has been used in a number of applications that are described. (19 Refs)
Subfile: C
Descriptors: parallel programming; programming environments
Identifiers: parallel programming systems; PRESTO; shared-memory multiprocessors; run-time kernel; object-oriented language C++; Sequence Balance 21000
Class Codes: C6115 (Programming support)

11/5/31 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

2017674 NTIS Accession Number: DE97005937
FLIC: A translator for same-source parallel implementation of regular grid applications
Michalakes, J.
Argonne National Lab., IL.
Corp. Source Codes: 001960000; 0448000
Sponsor: Department of Energy, Washington, DC.
Report No.: ANL/MCS-TM-223
Feb 97 15p
Languages: English
Journal Announcement: GRAI9722; ERA9737
Sponsored by Department of Energy, Washington, DC.

NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract No.: W-31109-ENG-38
FLIC, a Fortran loop and index converter, is a **parser** -based source translation **tool** that automates the conversion of program loops and array indices for distributed-memory **parallel computers** . This conversion is important in the implementation of gridded models on distributed memory because it allows for decomposition and shrinking of model data structures. FLIC does not provide the parallel services itself, but rather provides an automated and transparent mapping of the source code to calls or directives of the user's choice of run-time systems or parallel libraries. The amount of user-supplied input required by FLIC to direct the conversion is small enough to fit as command line arguments for the tool. The tool requires no additional statements, comments, or directives in the source code, thus avoiding the pervasiveness and intrusiveness imposed by directives-based preprocessors and parallelizing compilers. FLIC is lightweight and suitable for use as a precompiler and facilitates a same-source approach to operability on diverse computer architectures. FLIC is targeted to new or existing applications that employ regular gridded domains, such as weather models, that will be parallelized by data-domain decomposition.
Descriptors: *Array **Processors** ; * **Parallel** Processing; Computerized Simulation; F Codes; Iterative Methods; Mesh Generation; Translators
Identifiers: EDB/990200; NTISDE
Section Headings: 72GE (Mathematical Sciences--General)

11/5/33 (Item 4 from file: 6)
DIALOG(R)File 6:NTIS

1725347 NTIS Accession Number: AD-A262 425/2
Impact of Communication Style on Machine Resource Usage for the iWarp Parallel Processor
Gross, T. ; Hasegawa, A. ; Hinrichs, S. ; O'Hallaron, D. ; Stricker, T.
Carnegie-Mellon Univ., Pittsburgh, PA. Dept. of Computer Science.
Corp. Source Codes: 005343001; 403081
Report No.: CMU-CS-92-215
Nov 92 25p
Languages: English
Journal Announcement: GRAI9314
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract No.: MDA972-90-C-0035; ARPA ORDER-7330
Programs executing on a private-memory parallel system exchange data by explicitly sending and receiving messages. Two communication styles have been identified for such systems: memory communication (each message exchanged between two processors is buffered in memory, e.g. as in message passing) and systolic communication (each word of a message is transmitted directly from the sender processor to receiver processor, without any buffering in memory). The Warp system supports both communication styles and therefore provides a platform that allows us to evaluate how the choice of communication style impacts the usage of processor resources. Parallel program generators **map** a machine independent description of a computation onto a private-memory parallel system. We use two different parallel program generators that employ the two communication styles to **map** a set of application kernels onto iWarp. By using **tools** to **generate** the parallel programs, we are able to obtain realistic data on the execution of programs using the different communication styles. This paper reports on measurements of instruction format usage, the utilization of the communication ports (gates), and instruction frequencies on the iWarp system. It is a first step towards understanding how features and capabilities of **parallel processors** are actually used by parallel programs that have been **mapped** automatically.
Descriptors: ***Paralle l processors** ; *Computer communications; Computations; Formats; Generators; Impact; Instructions; Machines; Receivers; Resources; Computer programs; Message processing; Information transfer
Identifiers: NTISDODXA
Section Headings: 62B (Computers, Control, and Information Theory--Computer Software); 45C (Communication--Common Carrier and Satellite)

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Set     Items   Description
S1       9280   (CLUSTER OR PARALLEL)()(COMPUTER? OR PROCESSOR?) OR MMP OR
            SMP OR SHARED()MEMOR? OR MASPAR OR SIMD OR MP()(1 OR 2 OR ONE
            OR TWO)
S2    1643666   SCRIPT? OR TOOL? ? OR AGENT? OR MACRO OR MACROS OR JAVA OR
            JSCRIPT OR JVSCRIPT OR ACTIVEX OR ACTIVE()X OR SCENARIO? OR I-
            NSTRUCTION(N)(SET OR SETS)
S3      80677   PARSE? OR PARSING OR REPARS? OR MAP OR MAPPING OR TOKENI?
S4      85157   (GENERAT? OR CREAT? OR BUILD? OR ASSEMBL? OR AUTHOR OR WRI-
            TE)(2N)(IDENTICAL? OR SIMILAR? OR SAME? OR EQUAL OR EQUIVALEN-
            ?) OR CLONE? OR REPLICAT? OR DUPLICAT?
S5         49   S1 AND S2 AND S4
S6          4   S3 AND S5
S7         33   S1 AND S2 AND S3
S8         78   S5:S7
S9         42   S8 NOT AD=19990113:20010113
S10        13   S9 NOT AD=20010113:20030113
S11         9   S10 NOT AD=20030113:20050701
S12       276   S2 AND S4 AND (S1 OR PARALLEL?)
S13        19   S12 AND IC=(G06F OR H04L)
S14        15   S13 NOT S8
S15        11   S14 NOT AD=19990113:20010113
S16         6   S15 NOT AD=20010113:20030113
S17         6   S16 NOT AD=20030113:20050701
S18       158   S12 NOT AD=19990113:20010113
S19        11   S13 NOT AD=20010113:20030113
S20        12   S14 NOT AD=20030113:20050701
S21        21   S20 OR S17 OR S11
S22        21   IDPAT (sorted in duplicate/non-duplicate order)
S23        21   IDPAT (primary/non-duplicate records only)
S24     18035   S2(3N)(COPY OR COPIES OR CLONES OR REPLICATE? OR DUPLICATE?
            OR REPEAT? OR TWIN? OR PAIR? OR SECOND OR 2ND)
S25      1522   S2(3N)(BACKUP? OR BACK???()(UP OR UPS) OR DISTRIBUTED OR S-
            HARED)
S26        44   S1 AND (S24 OR S25)
S27       201   S26 OR S18
S28       188   S27 NOT AD=19990113:20010113
S29       123   S28 NOT AD=20010113:20030113
S30       107   S29 NOT AD=20030113:20050701
S31        16   S30 AND IC=(G06F OR H04L)
S32         8   S31 NOT S23
? show files
File 347:JAPIO Nov 1976-2005/Feb(Updated 050606)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200539
         (c) 2005  Thomson Derwent
```

32/5/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011816346 **Image available**
WPI Acc No: 1998-233256/199821
XRPX Acc No: N98-184850
Hardware simulator for transaction processing system - includes virtual hardware modules which write request to associated area of shared memory **and simulator** tools **which represents set of hardware devices**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CURRIE S; FLENLEY J M
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2319100	A	19980513	GB 9724061	A	19971115	199821	B
GB 2319100	B	19980916	GB 9724061	A	19971115	199839	
US 6275785	B1	20010814	US 98190752	A	19981112	200148	

Priority Applications (No Type Date): GB 9724061 A 19971115
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2319100	A		24	G06F-009/455	
GB 2319100	B			G06F-009/455	
US 6275785	B1			G06F-017/50	

Abstract (Basic): GB 2319100 A
The hardware simulator for a transaction processing system includes a set of virtual hardware modules which simulate the execution of transaction requests. The virtual hardware modules are responsive to transaction requests relayed from the transaction processing system, and are adapted to write the requests to an associated area of **shared memory** .
A simulator tool is adapted to graphically represent a set of hardware devices. Each hardware graphical representation is associated with an area of **shared memory** . The **tool** is adapted to monitor the area of **shared memory** and to update a hardware device graphical representation in response to a transaction request being written to an area of **shared memory** associated with the graphical representation.
USE - For simulating hardware for designing software for e.g. ATMs
ADVANTAGE - Allows new software to be developed without access to real hardware.
Dwg.6/9
Title Terms: HARDWARE; SIMULATE; TRANSACTION; PROCESS; SYSTEM; VIRTUAL; HARDWARE; MODULE; WRITING; REQUEST; ASSOCIATE; AREA; SHARE; MEMORY; SIMULATE; TOOL; REPRESENT; SET; HARDWARE; DEVICE
Derwent Class: T01
International Patent Class (Main): **G06F-009/455** ; **G06F-017/50**
International Patent Class (Additional): **G06F-009/44** ; **G06F-009/45** ; **G06F-013/10** ; G06G-007/62
File Segment: EPI

```
Set     Items   Description
S1       9280   (CLUSTER OR PARALLEL)()(COMPUTER? OR PROCESSOR?) OR MMP OR
            SMP OR SHARED()MEMOR? OR MASPAR OR SIMD OR MP()(1 OR 2 OR ONE
            OR TWO)
S2    1643666   SCRIPT? OR TOOL? ? OR AGENT? OR MACRO OR MACROS OR JAVA OR
            JSCRIPT OR JVSCRIPT OR ACTIVEX OR ACTIVE()X OR SCENARIO? OR I-
            NSTRUCTION(N)(SET OR SETS)
S3      80677   PARSE? OR PARSING OR REPARS? OR MAP OR MAPPING OR TOKENI?
S4      85157   (GENERAT? OR CREAT? OR BUILD? OR ASSEMBL? OR AUTHOR OR WRI-
            TE)(2N)(IDENTICAL? OR SIMILAR? OR SAME? OR EQUAL OR EQUIVALEN-
            ?) OR CLONE? OR REPLICAT? OR DUPLICAT?
S5         49   S1 AND S2 AND S4
S6          4   S3 AND S5
S7         33   S1 AND S2 AND S3
S8         78   S5:S7
S9         42   S8 NOT AD=19990113:20010113
S10        13   S9 NOT AD=20010113:20030113
S11         9   S10 NOT AD=20030113:20050701
S12       276   S2 AND S4 AND (S1 OR PARALLEL?)
S13        19   S12 AND IC=(G06F OR H04L)
S14        15   S13 NOT S8
S15        11   S14 NOT AD=19990113:20010113
S16         6   S15 NOT AD=20010113:20030113
S17         6   S16 NOT AD=20030113:20050701
S18       158   S12 NOT AD=19990113:20010113
S19        11   S13 NOT AD=20010113:20030113
S20        12   S14 NOT AD=20030113:20050701
S21        21   S20 OR S17 OR S11
S22        21   IDPAT (sorted in duplicate/non-duplicate order)
S23        21   IDPAT (primary/non-duplicate records only)
File 347:JAPIO Nov 1976-2005/Feb(Updated 050606)
        (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200539
        (c) 2005  Thomson Derwent
```

23/5/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011895798 **Image available**
WPI Acc No: 1998-312708/199827
Related WPI Acc No: 1998-274386; 1998-312695; 1998-312698; 1998-312706; 1998-312707; 1998-312709
XRPX Acc No: N98-245058

Distributed control method for structured data store - using globally addressable memory with control program resident on each network node which directs memory system to map **file and directory data into** shared memory **space**

Patent Assignee: MANGOSOFT CORP (MANG-N)
Inventor: CARTER J B; DAVIS S H; DIETTERICH D J; FRANK S J; LEE H H
Number of Countries: 079 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9822892	A1	19980528	WO 97US21466	A	19971121	199827 B
AU 9873035	A	19980610	AU 9873035	A	19971121	199843
EP 978069	A1	20000209	EP 97949572	A	19971121	200012
			WO 97US21466	A	19971121	
JP 2001506022	W	20010508	WO 97US21466	A	19971121	200131
			JP 98523946	A	19971121	
EP 978069	B1	20030618	EP 97949572	A	19971121	200341
			WO 97US21466	A	19971121	
DE 69722962	E	20030724	DE 622962	A	19971121	200356
			EP 97949572	A	19971121	
			WO 97US21466	A	19971121	

Priority Applications (No Type Date): US 97827534 A 19970328; US 96754481 A 19961122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9822892	A1	E	60	G06F-017/30	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW				
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9873035	A				Based on patent WO 9822892
EP 978069	A1	E			Based on patent WO 9822892
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE					
JP 2001506022	W		82	G06F-012/00	Based on patent WO 9822892
EP 978069	B1	E		G06F-017/30	Based on patent WO 9822892
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI NL PT SE					
DE 69722962	E			G06F-017/30	Based on patent EP 978069
					Based on patent WO 9822892

Abstract (Basic): WO 9822892 A

The method for structured data storage involves providing a number of nodes inter-connected by a network, and storing on each of the nodes an instance of a data control program for manipulating the structured store of data to provide multiple, distributed instances of the data control program. Each instance of the data control program is interfaced to a **shared memory** system that provides addressable persistent storage of data.

Each instance of the data control program is operated to use the **shared memory** system as a memory device having a structured store of data contained within it. The **shared memory** system therefore co-ordinates access to the structured store of data to provide distributed control over the structured store of data.

USE - Maintaining structured store of data, preferably within distributed, addressable, **shared memory** space storing data objects, **JAVA** applets and Web pages.

ADVANTAGE - Provides fault tolerant operation, and enables dynamic movement of data in response to network activity levels and access patterns, in order to optimise performance and minimise node times.

Dwg.1/11

Title Terms: DISTRIBUTE; CONTROL; METHOD; STRUCTURE; DATA; STORAGE; ADDRESS ; MEMORY; CONTROL; PROGRAM; RESIDENCE; NETWORK; NODE; DIRECT; MEMORY; SYSTEM; **MAP** ; FILE; DIRECTORY; DATA; SHARE; MEMORY; SPACE

Derwent Class: T01

International Patent Class (Main): G06F-012/00; G06F-017/30

International Patent Class (Additional): G06F-012/10

File Segment: EPI

23/5/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011470403 **Image available**
WPI Acc No: 1997-448310/199741
XRPX Acc No: N97-373670

Parallel processing computer for performing MIMD and SIMD operation - has global memory device from which instruction sets are received and duplicate copies of instruction sets are sent to each of first and second memory

Patent Assignee: ALACRON INC (ALAC-N)
Inventor: SGRO J A; STANTON P C
Number of Countries: 023 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9726593	A1	19970724	WO 97US497	A	19970110	199741	B
AU 9715772	A	19970811	AU 9715772	A	19970110	199747	
EP 875027	A1	19981104	EP 97902000	A	19970110	199848	
			WO 97US497	A	19970110		
US 5903771	A	19990511	US 96586066	A	19960116	199926	
			US 96619356	A	19960321		
AU 725592	B	20001012	AU 9715772	A	19970110	200055	

Priority Applications (No Type Date): US 96619356 A 19960321; US 96586066 A 19960116
Cited Patents: 2.Jnl.Ref; US 4481580; US 5430854
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9726593	A1	E	26	G06F-009/30	
Designated States (National): AU CA IL JP					
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
AU 9715772	A			G06F-009/30	Based on patent WO 9726593
EP 875027	A1	E		G06F-009/30	Based on patent WO 9726593
Designated States (Regional): CH DE FR GB LI NL					
US 5903771	A			G06F-015/00	Cont of application US 96586066
AU 725592	B			G06F-009/30	Previous Publ. patent AU 9715772 Based on patent WO 9726593

Abstract (Basic): WO 9726593 A

The system includes a first processor with a first inter-processor communication port device and a first memory interface. A second processor with a second inter-processor communication port device and a second memory interface. The first inter-processor communication port device is operatively connected to the second inter-processor communication port device.

The first memory device has a first port device operatively connected to the first memory interface and has a second port device in communication with a global memory device. A second memory has a third port operatively connected to the second memory interface and a fourth port in communication with the global memory. **Instruction sets** are received from the global memory device and **duplicate** copies of the **instruction sets** are sent to each of the first and second memory.

ADVANTAGE - Improves scaling capabilities. Makes efficient use of processor resources.

Dwg.1/6

Title Terms: PARALLEL; PROCESS; COMPUTER; PERFORMANCE; **SIMD** ; OPERATE; GLOBE; MEMORY; DEVICE; INSTRUCTION; SET; RECEIVE; **DUPLICATE** ; COPY; INSTRUCTION; SET; SEND; FIRST; SECOND; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-009/30; G06F-015/00
International Patent Class (Additional): G06F-013/28; G06F-015/80
File Segment: EPI

```
Set     Items   Description
S1      16661   (CLUSTER OR PARALLEL)()(COMPUTER? OR PROCESSOR?) OR MMP OR
             SMP OR SHARED()MEMOR? OR MASPAR OR SIMD OR MP()(1 OR 2 OR ONE
             OR TWO)
S2     691994   SCRIPT? OR TOOL? ? OR AGENT? OR MACRO OR MACROS OR JAVA OR
             JSCRIPT OR JAVASCRIPT OR APPLET OR JVSCRIPT OR ACTIVEX OR ACT-
             IVE()X OR SCENARIO? OR INSTRUCTION(N)(SET OR SETS)
S3     125066   PARSE? OR PARSING OR REPARS? OR MAP OR MAPPING OR TOKENI?
S4      40118   (GENERAT? OR BUILD? OR ASSEMBL? OR CREAT? OR WRITE OR REWR-
             IT? OR CLONE? OR REPLICAT? OR DUPLICAT? OR REPRODUC?)(3N)S2
S5          9   S1(10N)S3(S)S4
S6         37   S1(12N)S4
S7         94   S1(S)S3(S)S4
S8        129   S5:S7
S9         51   S8 NOT AD=19990113:20020113
S10        33   S9 NOT AD=20020113:20050701
S11        31   S10 AND IC=(G06F OR H04L)
S12        31   IDPAT (sorted in duplicate/non-duplicate order)
S13        31   IDPAT (primary/non-duplicate records only)
File 348:EUROPEAN PATENTS 1978-2005/Jun W02
         (c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050616,UT=20050609
         (c) 2005 WIPO/Univentio
```

13/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01165090
Method for simulating a data processing system having modules of more advanced versions
Verfahren zur Simulation eines Datenverarbeitunggssytems mit Modulen mit fortgeschrittenen Versionen
Methode pour simuler un systeme de traitement de donnees ayant des modules avec des versions avancees
PATENT ASSIGNEE:
BULL S.A., (244479), 68, route de Versailles, 78434 Louveciennes Cedex, (FR), (Applicant designated States: all)
INVENTOR:
Bosisio, Giuseppe, Via San Francesco d'Assisi, 52, 20099 Sesto San Giovanni - Milano, (IT)
LEGAL REPRESENTATIVE:
Pezzoli, Ennio et al (83661), Jacobacci & Perani S.p.A. Via Senato, 8, 20121 Milano, (IT)
PATENT (CC, No, Kind, Date): EP 1016993 A1 000705 (Basic)
APPLICATION (CC, No, Date): EP 98830805 981231;
DESIGNATED STATES: DE; FR; GB; IT
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-017/50**
ABSTRACT WORD COUNT: 170
NOTE:
Figure number on first page: 2B

LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200027	1059
SPEC A	(English)	200027	4859
Total word count - document A			5918
Total word count - document B			0
Total word count - documents A + B			5918

INTERNATIONAL PATENT CLASS: **G06F-017/50**

...SPECIFICATION levels), indicated by CM1, CM2, CM3, CM4 respectively, in which data (cache lines) of the **shared memory** 220 are **replicated** . The **agents** C1o-C4o, 215 and 225 are connected simultaneously (in what is called a slave mode...

13/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00897701
A multiprocessing system including an enhanced blocking mechanism for read-to-share-transactions in a NUMA mode
Multiprozessorsystem mit einem verbesserten Sperrmechanismus fur RTS-Transaktionen in NUMA-Modus
Systeme multiprocesseur avec un mecanisme ameliore de blocage pour transactions de type RTS en mode NUMA
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392730), 2550 Garcia Avenue, Mountain View, CA 94043, (US), (Applicant designated States: all)
INVENTOR:
Hagersten, Erik E., 3451 Cork Oak Way, Palo Alto, California 94303, (US)
Loewenstein, Paul N., 919 Channing Avenue, Palo Alto, California 94301, (US)
LEGAL REPRESENTATIVE:
Harris, Ian Richard et al (72231), D. Young & Co., 21 New Fetter Lane, London EC4A 1DA, (GB)
PATENT (CC, No, Kind, Date): EP 820016 A2 980121 (Basic)
EP 820016 A3 011024
APPLICATION (CC, No, Date): EP 97304597 970627;
PRIORITY (CC, No, Date): US 674271 960701
DESIGNATED STATES: DE; FR; GB; IT; NL; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-012/08**
ABSTRACT WORD COUNT: 94
NOTE:
Figure number on first page: 14

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 9804 746
SPEC A (English) 9804 15473
Total word count - document A 16219
Total word count - document B 0
Total word count - documents A + B 16219

INTERNATIONAL PATENT CLASS: **G06F-012/08**

...SPECIFICATION the transaction (if it is an LPA address) from the local physical address presented upon · **SMP** address bus 58 into the corresponding global address. Request **agent** 100 then **generates** a header packet specifying a particular coherency request to be transmitted to the home node...

...one embodiment, the coherency protocol enforced by request agents 100, home agents 102, and slave **agents** 104 includes a **write** invalidate policy. In other words, when a processor 16 within an **SMP** node 12 updates a coherency unit, any copies of the coherency unit stored within other...the coherency replies are received prior to the data phase of the write transaction upon **SMP** bus 20. Once the corresponding data has been received, request **agent** 100 transitions to **write** complete state 154. During write complete state 154, the coherency completion reply is transmitted to...clear block status state 176 upon receipt of a coherency completion not containing data.
Home **agent** 102 issues a **write** transaction upon **SMP** bus 20 during write data state 178 in order to transfer the received write data...

13/3,K/31 (Item 31 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00234265 **Image available**
SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE DECISION
Patent Applicant/Assignee:
STAR SEMICONDUCTOR CORPORATION,
Inventor(s):
ROBINSON Jeffrey I,
ROUSE Keith,
KRASSOWSKI Andrew J,
MONTLICK Terry F,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9308524 A1 19930429
Application: WO 92US8954 19921014 (PCT/WO US9208954)
Priority Application: US 91776161 19911015
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AU CA JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Publication Language: English
Fulltext Word Count: 219172

Main International Patent Class: **G06F-009/00**
International Patent Class: **G06F-09:40**
Fulltext Availability:
Claims

Claim
... microprocessor origins. In an attempt to overcome these limitations, attempts have been made to use **parallel processors** and math coprocessors. However, these "solutions" have required considerable expertise on the part of the...

...include speech and image recognition algorithms, disk drive controllers, speech generation algorithms, numerically controlled machine **tool** controllers,- etc. Based on the above break-down of tasks it can be seen that...for the data memory of the SPROC, and a symbol table which provides a memory **map** which maps variable names which the microprocessor will refer to
in separately compiling its program...bytes of microprocessor memory space. SPROC chip memory is 4K of 24-bit words that **map** to the microprocessor as 32-bit words. SMI supports applications using either Motorola-type (little...in C that include the SPROC chip. Such applications require, however, that one hardware memory **map** the SPROC.
E.3 The Development Process
The process required to develop a microprocessor application...

...into the applications work area; and create the microprocessor application. In addition, one must also **map** the SPROC chip(s) into the microprocessor's memory. It should be noted that aspects...code file locates the C variables at the appropriate places in the SPROC chip memory **map** . The symbol file generated by the SPROCbuild utility in the development system has the file...symbol file along with its symbol name, so that the symbol file comprises an address **map** of the symbol names for all nodes and attributes in the design. Some nodes and...Revision:
1.3 $11;
4-3 6
SUBSTITUTE SHEE'r

```
/* GLOBAL STORAGE for interfacing to  parser  and lexical anaLyser
char tmpree[MAXRL]; /* holds Latest identifier
char instrec[MAXRL],
specrec[MAXRL]; /* current...constants
types
data
static char exnode[] "$Revision: 1.3 $11;
/* GLOBAL STORAGE for interfacing to  parser  and Lexical anaLyser
char tmpree[MAXRL]; /* holds Latest identifier */
19
SUBSTITUTE SHEET
extern FILE *yyin...List[i])) != NULL)
*swap-char = sub-List[i+11;
/* end of make-vaLid-c-name */
/*  parse  name into series of dot-deLimited names, handle each name in
turn
/* ALL but the Lost name are nodes
void  parse -a
tine(char * symboL
rec)
I
char *start
ptr, *end-Ptr, *name;
node
type *item...symracZinterface(symboL rea);
insert(item, Whis List);
break; /* all. done with this record
end of  parsing  the Line
/* end of  parse .a.Line */
char interface2char(BOOLEAR interface)
return( (char)((interface) ? W
/* end of interface2char */
1* create...
```

Refine Search

Search Results -

Terms	Documents
L21 and L1	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L22

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 23, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L22	L21 and L1	0	L22
L21	L20 and execut$	13	L21
L20	L18 and pars$3	13	L20
L19	L18 and (parallel$5 near comput$6)	0	L19
L18	(L10 or L12 or L13) and L7	29	L18
L17	(L11 or L14 or L15 or L16) and L7	1	L17
L16	717/149.ccls.	175	L16
L15	717/119.ccls.	30	L15
L14	717/115.ccls.	125	L14
L13	717/$.ccls.	8723	L13
L12	709/$.ccls.	37243	L12
L11	709/217-219.ccls.	6734	L11
L10	707/$.ccls.	27516	L10
L9	L8 and (parallel$5 near comput$6)	1	L9

L8	L7 and execut$	92	L8
L7	("script driven") or (script near driven)	101	L7
L6	L5 and (("script driven") or (script near driven))	0	L6
L5	L4 and L1	35	L5
L4	L3 and L2	589	L4
L3	pars$3 same script	2040	L3
L2	script near execut$	4079	L2
L1	parallel$5 same (application near program$)	6273	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L8 and (parallel$5 near comput$6)	1

1-24
6-23-05

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L9

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Thursday, June 23, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L9	L8 and (parallel$5 near comput$6)	1	L9
L8	L7 and execut$	92	L8
L7	("script driven") or (script near driven)	101	L7
L6	L5 and (("script driven") or (script near driven))	0	L6
L5	L4 and L1	35	L5
L4	L3 and L2	589	L4
L3	pars$3 same script	2040	L3
L2	script near execut$	4079	L2
L1	parallel$5 same (application near program$)	6273	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: JP 2003529808 W, WO 200042518 A1, AU 200026126 A, EP 1228439 A1

L9: Entry 1 of 1 File: DWPI Oct 7, 2003

DERWENT-ACC-NO: 2000-679129
DERWENT-WEEK: 200370

TITLE: Script driven software tool parallelization method e.g. SAS software system, involves producing parallel computation specification and script fragment based on analysis of script

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

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Terms	Documents
L8 and (parallel$5 near comput$6)	1

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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G06F 15/00, 15/62, 17/30

A1

(11) International Publication Number: **WO 00/42518**

(43) International Publication Date: 20 July 2000 (20.07.00)

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(22) International Filing Date: 13 January 2000 (13.01.00)

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09/229,849 13 January 1999 (13.01.99) US

(71) Applicant: AB INITIO SOFTWARE CORPORATION [US/US]; 201 Spring Street, Lexington, MA 02421 (US).

(72) Inventor: SERRANO, Martin; AB Initio Software Corporation, 201 Spring Street, Lexington, MA 02421 (US).

(74) Agent: LAND, John; Fish & Richardson, P.C., Suite 1400, 4225 Executive Square, La Jolla, 92037 (US).

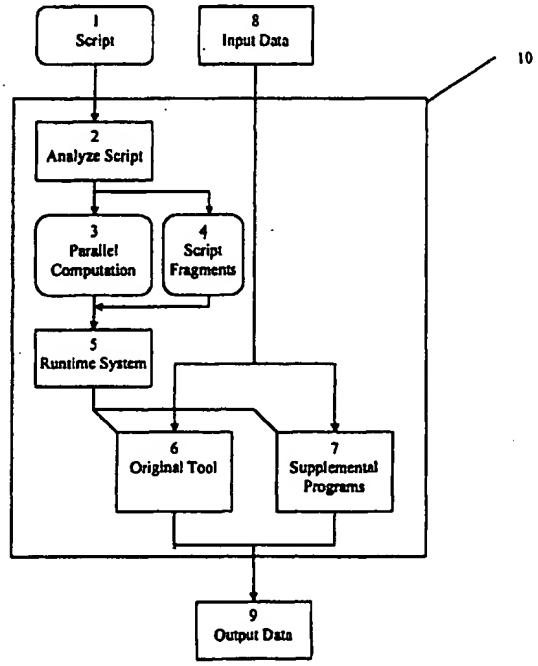
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: PARALLELIZING APPLICATIONS OF SCRIPT-DRIVEN TOOLS

(57) Abstract

A system and method for parallelizing applications of script-driven software tools. Scripts in the software tool scripting (1) language are automatically analyzed (2) in order to produce a specification for a parallel computation (3) plus a set of "script fragments", the combination of which is functionally equivalent to the original script. The computational specification plus the script fragments (4) are then executed by a parallel runtime system (5), which causes multiple instances of the original software tool (6) and/or supplemental programs (7) to be run as parallel processes. The resulting processes will read input data (8) and produce output data (9), performing the same computation as was specified by the original script. The combination of the analyzer (2), runtime (5), original software tool, and supplemental programs will, for a given script and input data, produce the same output data as the original software tool alone, but has the capability of using multiple processors in parallel for substantial improvements in overall "throughput". The invention includes computer program embodiments of an automatic script analyzer.



Refine Search

Search Results -

Terms	Documents
L5 and (("script driven") or (script near driven))	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5 and (("script driven") or (script near driven))	0	L6
L5	L4 and L1	35	L5
L4	L3 and L2	589	L4
L3	pars$3 same script	2040	L3
L2	script near execut$	4079	L2
L1	parallel$5 same (application near program$)	6273	L1

END OF SEARCH HISTORY

L8: Entry 20 of 21 File: USPT Aug 22, 2000

DOCUMENT-IDENTIFIER: US 6108685 A
TITLE: System for generating periodic reports generating trend analysis and intervention for monitoring daily living activity

Detailed Description Text (73):
Using this data from the user monitoring system 100, the remote case monitoring system 148 may provide on-line case monitoring of each user by receiving standard information and information designated as priority information and analyzing the received information. In order to do this, the remote case monitoring system 148 converts incoming data on each user into various summary reports which track the activities of the client. This makes it possible to distribute specialized gerontological every day living summary reports to users, family members, case managers, physicians and others. It also makes it possible to collect and act upon the designated priority information which may indicate immediate problems for the user. For example when a user appears not to have gotten out of bed a problem may be indicated.

Current US Original Classification (1):
709/200

CLAIMS:

1. A system for monitoring a user in a user living area, said system including a remote monitoring site comprising;

a system controller;

an activity detection subsystem decoupled from the user for monitoring a daily living activity of said user independently of physiological measurements, said activity detection subsystem having at least one detector device capable of being activated in response to an occurrence of said daily living activity and capable of determining at said user living area that said daily activity has occurred to provide information to said system controller representative of said daily living activity, said system controller having a control circuit for generating a control signal in response to said information representative of said daily living activity;

a control information communication channel for applying said control signal to said remote monitoring site;

a report generator for generating a scheduled periodic report on said daily living activity, said report having collections of said information representative of a selected daily living activity; and

circuitry for intervening in said user living area in accordance with said scheduled periodic report.

6. The system of claim 1, wherein the report generator is disposed at the user living area.

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e-mail

Results for "(('script-driven') <paragraph> execut* <paragraph> parallel* <and> pars*)<in..."
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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(('script-driven') <paragraph> execut* <paragraph> parallel* <and> pars*)<in>metada

Check to search only within this results set

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No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

Results for "((('script-driven') <near> ('software tool')) <and> execut* <and> parallel*)&..." e-mail

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((('script-driven') <near> ('software tool')) <and> execut* <and> parallel*)<in>metada

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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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11746
6-23-05

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IEEE JNL	IEEE Journal or Magazine
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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

((('script driven') <near> ('software tool')) <and> execut* <and> parallel*)<in>metada

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No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

Indexed by Inspec

10-13-05

IEEE Xplore RELEASE 2.0

Results for "(((script <near> driven) <paragraph> (software <near> tool) <and> execut* &l..."

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Your search matched 0 of 1174497 documents.

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(((script <near> driven) <paragraph> (software <near> tool) <and> execut* <and> par

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Indexed by Inspec

Terms used **script driven executed parallel parsing script** Found **1** of **157,956**

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1 Visualizing the behavior of object-oriented systems

Wim De Pauw, Richard Helm, Doug Kimelman, John Vlissides

October 1993 **ACM SIGPLAN Notices , Proceedings of the eighth annual conference on Object-oriented programming systems, languages, and applications**, Volume 28 Issue 10

Full text available: pdf(1.57 MB) Additional Information: full citation, references, citings, index terms

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Terms used **script driven executed parallel analyzing script parsing script**

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Relevance scale

1 Papers: Analysis of errors in network load measurements

Stanislav Belenki, Sven Tafvelin

January 2000 **ACM SIGCOMM Computer Communication Review**, Volume 30 Issue 1

Full text available: pdf(750.73 KB) Additional Information: full citation, abstract, references

The paper identifies elements in network monitoring systems that cause errors in the load measurements found in recent reports on network statistics from an academic backbone network. Two types of network monitors are investigated: counter-based and packet capturing. The paper explains how to assign an accuracy term to the load values in case of counter-based monitors and how to eliminate distortion in the case of packet capturing monitors. The paper also suggests an MIB to reduce the counter-ba ...

2 Visualizing the behavior of object-oriented systems

Wim De Pauw, Richard Helm, Doug Kimelman, John Vlissides

October 1993 **ACM SIGPLAN Notices , Proceedings of the eighth annual conference on Object-oriented programming systems, languages, and applications**, Volume 28 Issue 10

Full text available: pdf(1.57 MB) Additional Information: full citation, references, citings, index terms

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Terms used **script driven software tool executed parallel analyzing script parsing script dataset definitions**

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Relevance scale

1 The instrumentation of multics

Jerome H. Saltzer, John W. Gintell

August 1970 **Communications of the ACM**, Volume 13 Issue 8

Full text available: pdf(798.48 KB) Additional Information: full citation, abstract, references, citings

An array of measuring tools devised to aid in the implementation of a prototype computer utility is discussed. These tools include special hardware clocks and data channels, general purpose programmed probing and recording tools, and specialized measurement facilities. Some particular measurements of interest in a system which combines demand paging with multiprogamming are described in detail. Where appropriate, insight into effectiveness (or lack thereof) of individual tools is provided.< ...

Keywords: demand paging, event tracing, instrumentation, measuring tools, metering, multics, multiprogramming systems, performance measurement, script driven measurement, system analysis

2 Instrumentation and measurement: The instrumentation of multics

Jerome H. Saltzer, John W. Gintell

October 1969 **Proceedings of the second symposium on Operating systems principles**

Full text available: pdf(779.73 KB) Additional Information: full citation, abstract, references

This paper reports an array of measuring tools devised to aid in the implementation of a prototype computer utility. These tools include special hardware clocks and data channels, general purpose programmed probing and recording tools, and specialized measurement facilities. Some particular measurements of interest in a system which combines demand paging with multi-programming are described in detail. Where appropriate, insight into effectiveness (or lack thereof) of individual tools is provide ...

3 The user interface and program structure of a graphical VLSI layout editor

Kevin S. B. Szabó, Mohamed I. Elmasry

May 1986 **ACM SIGCHI Bulletin , Proceedings of the SIGCHI/GI conference on Human factors in computing systems and graphics interface**, Volume 17 Issue SI

Full text available: pdf(585.97 KB) Additional Information: full citation, abstract, references, index terms

In this paper the user interface and program organization of the SYMPLE VLSI symbolic layout editor is examined. The user interface is driven by a small interpreter that is

constructed from a LISP-like language at run time and has access to a consistent library of menus and graphical information-gathering functions. To improve maintainability, the editor has been constructed in a modular form with well-defined interfaces.

Keywords: CAD/CAM, VLSI editor, symbolic layout, user interface

4 Visualizing the behavior of object-oriented systems

Wim De Pauw, Richard Helm, Doug Kimelman, John Vlissides

October 1993 **ACM SIGPLAN Notices , Proceedings of the eighth annual conference on Object-oriented programming systems, languages, and applications**, Volume 28 Issue 10

Full text available: pdf(1.57 MB) Additional Information: full citation, references, citings, index terms

Results 1 - 4 of 4

Terms used **script driven executed parallel analyzing script parsing script dataset**

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Relevance scale

1 The utility of exploiting idle workstations for parallel computation

Anurag Acharya, Guy Edjlali, Joel Saltz

June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1

Full text available: pdf(1.73 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we examine the utility of exploiting idle workstations for parallel computation. We attempt to answer the following questions. First, given a workstation pool, for what fraction of time can we expect to find a cluster of *k* workstations available? This provides an estimate of the opportunity for parallel computation. Second, how stable is a cluster of free machines and how does the stability vary with the size of the cluster? This indicates how frequently a parallel computat ...

2 Analysis methodology: Simulation output analysis: truncation point estimation using multiple replications in parallel

Falko Bause, Mirko Eickhoff

December 2003 **Proceedings of the 35th conference on Winter simulation: driving innovation**

Full text available: pdf(399.94 KB) Additional Information: full citation, abstract, references

In steady-state simulation the output data of the transient phase often causes a bias in the estimation of the steady-state results. A common advice is to cut off this transient phase. Finding an appropriate truncation point is a well-known problem and is still not completely solved. In this paper we consider two algorithms for the determination of the truncation point. Both are based on a technique which takes the definition of the steady-state phase more closely into consideration. The capa ...

3 Dynamic adaptation to available resources for parallel computing in an autonomous network of workstations

Umit Rencuzogullari, Sandhya Dwardadas

June 2001 **ACM SIGPLAN Notices , Proceedings of the eighth ACM SIGPLAN symposium on Principles and practices of parallel programming**, Volume 36 Issue 7

Full text available: pdf(344.17 KB) Additional Information: full citation, abstract, references, citings, index terms

Networks of workstations (NOWs), which are generally composed of autonomous compute elements networked together, are an attractive parallel computing platform since they offer

high performance at low cost. The autonomous nature of the environment, however, often results in inefficient utilization due to load imbalances caused by three primary factors: 1) unequal load (compute or communication) assignment to equally-powerful compute nodes, 2) unequal resources at compute nodes, and 3) multip ...

4 MPICH-V: toward a scalable fault tolerant MPI for volatile nodes

George Bosilca, Aurelien Bouteiller, Franck Cappello, Samir Djilali, Gilles Fedak, Cecile Germain, Thomas Herault, Pierre Lemarinier, Oleg Lodygensky, Frederic Magniette, Vincent Neri, Anton Selikhov

November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: pdf(204.28 KB) Additional Information: full citation, abstract, references, citings, index terms

Global Computing platforms, large scale clusters and future TeraGRID systems gather thousands of nodes for computing parallel scientific applications. At this scale, node failures or disconnections are frequent events. This Volatility reduces the MTBF of the whole system in the range of hours or minutes.We present MPICH-V, an automatic Volatility tolerant MPI environment based on uncoordinated checkpoint/rollback and distributed message logging. MPICH-V architecture relies on Channel Memories, C ...

5 Papers: Analysis of errors in network load measurements

Stanislav Belenki, Sven Tafvelin

January 2000 **ACM SIGCOMM Computer Communication Review**, Volume 30 Issue 1

Full text available: pdf(750.73 KB) Additional Information: full citation, abstract, references

The paper identifies elements in network monitoring systems that cause errors in the load measurements found in recent reports on network statistics from an academic backbone network. Two types of network monitors are investigated: counter-based and packet capturing. The paper explains how to assign an accuracy term to the load values in case of counter-based monitors and how to eliminate distortion in the case of packet capturing monitors. The paper also suggests an MIB to reduce the counter-ba ...

6 Visualizing the behavior of object-oriented systems

Wim De Pauw, Richard Helm, Doug Kimelman, John Vlissides

October 1993 **ACM SIGPLAN Notices , Proceedings of the eighth annual conference on Object-oriented programming systems, languages, and applications**, Volume 28 Issue 10

Full text available: pdf(1.57 MB) Additional Information: full citation, references, citings, index terms

7 Interactive manipulation and display of surfaces in four dimensions

David Banks

June 1992 **Proceedings of the 1992 symposium on Interactive 3D graphics**

Full text available: pdf(2.99 MB) Additional Information: full citation, references, citings, index terms

Results 1 - 7 of 7